Technical Schedule of IEEE EDKCON 2018			
Day-1 (24.11.2018)		Day-2 (25.11.2018)	
8.00 am-9.00 am	Registration	8.00 am-9.00 am	Registration
8.30 am-9.00 am	Tea/Snacks	8.30 am-9.00 am	Tea/Snacks
9.00 am - 9.40 am	Inauguration Program	9.00 am - 9.30 am	Technical Talk by Prof. J. K. Mandal, India
9.40 am-10.30 am	Plenary Talk by Prof. Vijay K. Arora, IEEE EDS DL, USA	9.30 am-10.10 am	Key-note Talk by Prof. Ajit Kr. Panda, IEEE EDS DL , India
10.30 am-11.20 am	Plenary Talk by Prof. Anisul Haque, IEEE EDS DL , Bangladesh	10.10 am-10.50 am	Key-note Talk by Prof. Subir Kr. Sarkar, IEEE EDS DL , India
11.20 am - 12.00 pm	Key-note Talk by Prof. Manoj Saxena, IEEE EDS DL , India	10.50am-11.20 am	Technical Talk by Prof. Rakesh Vaid, India
12.00 pm-12.50 pm	Plenary Talk by Prof. Li Wei Ko, Taiwan	11.20 pm-01.20pm	Track-7 :Process and Manufacturing Technology (ED32, ED123, ED12, ED90, ED89, ED101, ED57, ED30, ED120, ED82)
12.50 pm - 1.30 pm	Key-note Talk by Prof. Yogesh SIngh Chauhan, IEEE EDS DL , India		Track-8 :Device Modelling and Simulation-III (ED88, ED39, ED111, ED97, ED55, ED18, ED3, ED117, ED26, ED25)
01.30 pm - 02.00 pm	Lunch		Track-9 :Device Modelling and Simulation-IV (ED114, ED10, ED50, ED106, ED96, ED87, ED93, ED14,ED17, ED42)
02.00 pm - 02.40pm	Key-note Talk by Prof. G. N. Dash, IEEE EDS DL , India	01.20 pm - 02.00 pm	Lunch
02.40 pm-04.15pm	Track-1 :Emerging Device-I (ED104, ED85, ED75, ED61, ED36, ED121, ED15)	02.00 pm - 04.00 pm	Track-10 :Emerging Devices-II (ED83, ED70, ED29, ED80, ED56, ED48, ED11, ED60, ED13, ED119, ED40)
	Track-2 :Device Modelling and Simulation-I (ED63, ED62, ED23, ED43, ED59, ED99,ED73)		Track-11 :Photovoltaic & Photonic Device (ED81, ED79, ED53, ED44, ED35, ED1, ED86, ED5, ED77, ED49, ED46)
	Track-3 :High Speed Device/HEMT (ED95, ED74, ED68, ED67, ED103, ED124,ED37)		Track-12 :Device Modelling and Simulation-V (ED110, ED52, ED58, ED69, ED38, ED71, ED41, ED78, ED16, ED100, ED94)
04.15 pm - 04.30 pm	Tea/Snacks	04.00 pm-04.15 pm	Tea/Snacks
04.30 pm - 06.00 pm	Track-4 :Sensing Devices (ED64, ED118, ED24, ED22, ED8, ED125)	4.15 pm - 05.45 pm	Track-13 :MEMS/NEMS-II (ED6, ED4, ED105, ED84, ED2, ED9, ED127)
	Track-5 :MEMS/NEMS-I (ED107, ED92, ED76, ED21, ED19, ED65, ED129)		Track-14 :Circuit and Device Interactions (ED102, ED116, ED51, ED33, ED20, ED47, ED45)
	Track-6 :Device Modelling and Simulation-II (ED34, ED31, ED7, ED113, ED112, ED98, ED130)		Track-15 :Embedded Devices (ED126, ED128, ED28, ED72, ED122, ED54, ED115)
			Track-16: Emerging Device-II (ED27, ED66, ED109, ED108, ED91, ED131, ED132)
		5.45pm-06.00 pm	Valedictory Session

Track 1: Emerging Device-I	
ED104	Parametric Variation of ZnSe/TiO2 Electron Transport Layer Based Perovskite Solar Cell: A Simulation Study and Optimization
ED85	Numerical Simulation of CeOX ETL Based Perovskite Solar Cell:- An Optimization Study for High Efficiency and Stability
ED75	Performance Enhnaced Unsymmetrical FinFET and its Applications
ED61	RingFET Architecture for High Frequency Applications: TCAD based Assessment
ED36	Stress Tuning in NanoScale FinFETs at 7nm
ED121	High performance Low leakage pocket SixGe1-x Junction-less Single-GateTunnel FET for 10 nm Technology
ED15	Effect of InGaAsP Cap-layer in InP/InGaAs pnp Î´-doped Heterojunction Bipolar Transistor
Track 2:Device Modelling and Simulation-I	
ED63	Sub-threshold Drain Current Model of Shell-Core Architecture Double Gate JunctionLess Transistor
ED62	Studying the Impact of Compound Semiconductor Material in Drain Region Extended Tunnel Transistor for SoC Applications
ED23	Study of Gate Misalignment effects in Single-Material Double-Gate (SMDG) MOSFET Considering source and drain Lateral Gaussian Doping Profile
ED43	Analysis of Interface Trap Charges of Double gate Junctionless Nanowire Transistor (DG-JNT) for Digital Circuit Applications
ED59	OXIDE STACK ENGINEERED DOUBLE SURROUNDING GATE (OSE-DSG) MOSFET FOR SUBMILLIMETER ANALOG APPLICATION
ED99	A Multi Vt Approach for Silicon Nanotube FET with Halo Implantation for Improved DIBL
ED73	Incorporation of Tensile and Compressive channel Stress by Modulating SiGe Stressor length in Embedded Source/Drain Si-FinFET Architecture
Track 3: High Speed Device/HEMT	
ED95	Impact of variation in barrier thickness on a Gate-Engineered TM-DG Heterostructure MOSFET to suppress SCEâ€™s and itâ€™s Analog,RF,linearity performance investigation for SOC applications.
ED74	Impact of donor layer thickness, doping concentration and gate-width on Gate-Capacitance of AlGaN/GaN Single and Double Heterostructure HEMT for Microwave Frequency Applications
ED68	DC and RF Characterization of InAs based Double delta doped MOSHEMT device
ED67	Noise Characterisation of InAs Based DG-HEMT Devices for RF Applications
ED103	Capacitive Analysis of Hetero Material Gate PNIN-DG-TFET over Diverge Temperature Range for Superior RF/Microwave Performance
ED124	Stepped poly gate In0.53Ga0.47As/InP MOSHFET to enhance the device Performance
ED37	Stress Analysis in Uniaxially Strained-SiGe Channel FinFETs at 7N Technology Node
Track 4: Sensing Devices	

ED64	Device Modeling of Double Layered TiO2 Nanotube Array based Resistive Vapor Sensor
ED118	Dielectric Modulated Triple Metal Gate All Around MOSFET (TMGAA) for DNA Bio-Molecule Detection
ED24	Improvement of Acetone Sensing Performance in rGO Modified ZnO Nanotubes based Binary Hybrid Structure at Low Temperature
ED22	An Efficient Microsensor System for Selective Detection of Methanol using TiO2 Nanotubes
ED8	Study of Ag doped SnO2 film and its response towards aromatic chemicals present in tea
ED125	Comparative Study of Unmodified WO3-ZnO and Au-Modified WO3-ZnOBased thin film Sensor Fabrication for Enhanced CH4 Gas Sensing Performance
Track 5: MEMS/NEMS-I	
ED107	Performance Analysis of RF MEMS switch having Serpentine Flexure design for High Isolation and Low Pull-in voltage
ED92	Design of CPW based Tunable RF MEMS Band Pass Filter
ED76	Design of Real-Time Acquisition and Filtering for MEMS-based Accelerometer Data in Microcontroller
ED21	Low loss ohmic type piezoelectric actuated RF MEMS switch designed with PZT and ZnO
ED19	Design Optimization of Micro Disk Resonator Using Interior Point Algorithm
ED65	Nano Structured Gas Sensing Device and Its Application in Underground Mines
ED129	Design of 6nm MOSFET and its Applications
Track 6: Device Modelling and Simulation-II	
ED34	Analysis of miniaturized acoustic transducer for cell-lysis
ED31	Calibration and Pre-Processing Techniques for A Smartphone-Based Driving Events Identification and Classification System
ED7	An extensive simulation study of gaussian drain doped heterojunction double gate TFET
ED113	An Impact of the Voltage & Current Ripples in the Power Stages of the Boost Converter
ED112	Mathematical Analysis and simulation for designing two Dimensional out pipe Crawler for Oil Industry
ED98	A Review On The Effects Of Technology On CMOS and CPL Logic Style On Performance, Speed And Power Dissipation
ED130	Electrical Characteristics Assessment of Gate Metal and Source Pocket Engineered DG-TFET for low Power Analog Applications
Track 7: Process and Manufacturing Technology	
ED32	Wettability of Metal Assisted Chemically Etched (MaCE) Grass like Silicon Nanowires
ED123	Effect of process temperature on molybdenum disulphide layers grown by chemical vapor deposition technique

ED12	Low Temperature and Highly Selective H2 Sensing System using WO3-ZnO Heterostructure Decorated with Pd Nanoparticle
ED90	Automation of 14.5 GHz ECR ion source and injection line distributed vacuum system for room temperature cyclotron
ED89	Crystallographic growth pattern of well-ordered â€œripple-shapedâ€ microstructures on Mn thin films
ED101	Effect of various dielectrics to plasmonic improvement in metal-dielectricâ€“semiconductor substrate
ED57	Dye-Sensitized Solar Cells Fabrication Employing Natural hues as Photosensitizing Substances
ED30	Investigations on Infrared(IR) Sensitive Material for Microbolometer using Material Selection Approaches
ED120	Thermal and Optoelectrical analysis of La0.7Sr0.3MnO3 Thin Film Thermistor in 8-12 Âµm range for Uncooled Microbolometer Application
ED82	Multi-layered Thermal Actuator realization using Metal Passivated TMAH Micro-machining
Track 8: Device Modeling and Simulation -III	
ED88	Performance analysis of Schottky Barrier height modulation in strained (10, 0) MoS2 Armchair Nano Ribbon-metal junction
ED39	Gate-All-Around Si-Nanowire Transistors:Simulation at Nanoscale
ED111	A Study on sensitivity of ION/IOFF ratio of JLT to structural parameters
ED97	PERFORMANCE ANALYSIS OF DOWN SCALING EFFECT OF Si BASED SRG TUNNEL FET
ED55	Comparison of electrical characteristics of 28 nm Bulk MOSFET and FDSOI MOSFET
ED18	Impact of Device Parameters on the Threshold Voltage of Double-Gate, Tri-Gate and Gate-All-Around MOSFETs
ED3	Modeling short channel behavior of proposed Work Function Engineered High-k gate stack DG MOSFET with vertical Gaussian doping
ED117	Effect of strain on Density of States and Directional Dependent Electron Effective Mass of two dimensional intrinsic Graphene
ED26	Effect of High-K Dielectric on Drain Current of ID-DG MOSFET using Ortiz-Conde Model
ED25	Analytical Investigation of Differential Conductance in Submicron HEMT with Two Different Substrates
Track 9: Device Modeling and Simulation -III	
ED114	A Selective Harmonic Elimination (SHE) Technique For the Multi-Leveled Inverters
ED10	Novel Approach to Design DPL-based Ternary Logic Circuits
ED50	ON SOME ANALYSIS OF OPTICAL MICRORING RESONATOR TO THE GENERATION OF MICROWAVE SIGNAL
ED106	Design of Flyback Converter by using an Ideal Switch and a MOSFET Switch

ED96	COMPARISION OF LINEARITY PERFORMANCE OF InP BASED DGMOSFETS WITH GATE STACK ,SiO2 AND HfO2
ED87	Enhanced modified Smith predictor for delay dominated unstable processes
ED93	STUDY OF EFFECT OF DOWN SCALING ON THE ANALOG/RF PERFORMANCE OF GATE ALL AROUND JLMOSFET
ED14	Study on Impact of LC-Filter Parameters under Variable Loading Conditions of Three-Phase Voltage Source Inverter
ED17	Third Order Sinusoidal Oscillator employing single CCDDCCTA
ED42	Study of Power Delay Characteristic of Sub-threshold SCL inverter using Junction-less DG-MOSFET
Track 10: Emerging Device-II	
ED83	Two Strained-Si layers in Channel region of HOI MOSFET
ED70	Tuning of bandstructure of single-walled carbon nanotube functionalized with ssDNA oligonucleotide sequence
ED29	Semi-Empirical Modeling of electrically doped Graphene Nanoribbon Field Effect Transistor
ED80	Analysis of Different Gate Dielectric Materials in Carbon Nanotube Field Effect Transistor (CNFET) using Optimization Technique
ED56	Dual-Metal Graded-Channel Double-Gate Tunnel FETs for Reduction of Ambipolar Conduction
ED48	A Hybrid Atomistic â€“ Semi-analytical modeling on Schottky barrier Au-MoS2-Au MOSFETs
ED11	Performance assessment of a double gate work function engineered doped Tunnel FET based on 2D surface potential model
ED60	Effect of strain on Quantum Capacitance of two dimensional intrinsic Graphene
ED13	Design, Simulation and Optimisation of an Arrayed Gas Sensor using Metal Oxide based Nanowires
ED119	Dependency of fT and fMAX on various Device Parameters of AlGaN/GaN HEMT
ED40	Power and Delay Analysis of Junction-less Double Gate CMOS Inverter in Near and Sub-threshold Regime
Track 11: Photovoltaic & Photonic Devices	
ED81	Multilayer Graphene Oxide as an Active Layer in Silicon Heterojunction Solar Cell
ED79	Si~3C-SiC Multiple Quantum Barrier High Speed, Wide-Band Avalanche Photodiodes
ED53	Numerical Modeling Of Native Defects in CVD Grown Diamond Photodetectors
ED44	Analysis of Tera Hertz Optical Asymmetric Demultiplexer(TOAD) based Optical Switch using soliton pulse
ED35	A Simulation Based Comparative Study of P3HT: PCBM and OC1C10PPV: PCBM Organic Solar Cells
ED1	Optimization of the components of a Visible light communication system for efficient data transfer
ED86	Prediction of Effective Core Area and Index of Refraction of Single-mode Graded Index Fiber in Presence of Kerr Nonlinearity

ED5	Effect of Intersubband Interaction on Non-linear Electron Mobility in Asymmetric AlGaAs Parabolic Double Quantum Well Structure
ED77	Electron transport in AlxGa1-xAs based non-square double quantum well field effect transistor structure
ED49	Multiple Quantum Well IMPATT source based on Si~3C~SiC Heterostructure operating at Millimeter-wave and Terahertz Frequency Band
ED46	Effect of High-K Dielectric on the Performances of Adiabatic Logic Circuits in Sub-threshold Regime
Track 12: Device Modelling and Simulation-IV	
ED110	Analysis of Different Characteristics of SOI-TFET with Ge Material as Source Pocket
ED52	Analysis of low frequency noise in nanoscale InAsxSb1-x MOSFETs with varying compositions
ED58	Breakdown Voltage Analysis of Different Field Plate AlGaN/GaN HEMTs : TCAD Based Assesment
ED69	EFFECT OF CHANNEL DIMENSION ON TRANSFORMER CHARACTERISTICS OF GRAPHENE FET
ED38	Stability performance comparison of a MTJ memory device using low-dimensional HfO2, Al2O3, La2O3 and h-BN as composite dielectric
ED71	Impact of Source Engineering in Split Drain Tunnel Field Effect Transistor
ED41	Variability Due to Orientation Dependent Oxide Thickness in SOI-FinFETs
ED78	Ambipolar performance improvement of dual material TFET using drain underlap engineering
ED16	Simulation based performance analysis of a double gate work function engineered doped Tunnel FET
ED100	Modeling of carbon chain device employing quantum mechanical method: A hybrid diode
ED94	Analytical Modeling of Drain Current of Junctionless Double Gate Si-MOSFET having Variable Barrier Height Considering Band Non-Parabolicity
Track 13: MEMS/NEMS II	
ED6	Experimental Investigation of load Characteristics of Piezofilm-based Energy Harvestert
ED4	Inadequacy of Markov Model in Modelling of Electromigration -induced Resistance Degradation
ED105	An Investigation on Capacitance Modeling of RF MEMS Perforated Shunt Switch
ED84	Design and fabrication of Electro-Thermal 1-D Micro-Mirror
ED2	Investigation of Design Parameters in MEMS Based Piezoelectric Vibration Energy Harvester
ED9	Millimeter-wave and Terahertz Magnetic Field Avalche Transit Time Sources
ED127	Small Signal Modeling of Charge Plasma Based Cylindrical/Surrounding Gate MOSFET for RF Application Incorporating Fringing Effect
Track 14: Circuit and Device Interactions	

ED102	Optimizing Fin Aspect Ratio of Junctionless bulk FinFET for Application in Analog/RF Circuit
ED116	Run Time Vth Extraction Based On-chip NBTI Mitigation Sensor for 6T SRAM Cell
ED51	Design and analysis of a low power high performance GDI based radix 4 multiplier using modified Booth Wallace algorithm
ED33	A novel GaN-HEMT based inverter and cascode amplifier
ED20	Quantum Cost Optimized Design of Reversible 2's Complement Code Converter
ED47	FPGA Implementation of RNS Adder Based MAC Unit in Ternary Value Logic Domain for Signal Processing Algorithm and its Performance Analysis
ED45	Analytical study of unipolar junction transistor as a novel dual material double gate MOSFET to suppress short-channel effect
Track 15: Embedded Devices	
ED126	Energy-efficient approximate squaring hardware for error-resilient digital systems
ED128	Power-Energy Optimization of Solar Photovoltaic Device Modeling
ED28	A Vector File Generation Program for Simulating Single Electron Transistor Based Computing System
ED72	PSO Variants and Its comparison with Firefly Algorithm in solving VLSI Global Routing Problem
ED122	FPGA realization of Medical Image Watermarking
ED54	Design and implementation of highly secured arduino based voting machine
ED115	Effect of Band Parabolicity on Energy Sub-Band Profile for Nano-Dimensional Junctionless Metal Oxide Semiconductor Field Effect Transistors.
Track 16: Emerging Device-III	
ED27	Resistive switching behavior of RF sputtered calcium copper titanate thin films with various annealing approach
ED66	Design of MEMS Temperature sensor using Molybdenum Material for Enhancing its Performance
ED109	Electrochemical analysis of Graphene oxide and Reduced Graphene Oxide for Super Capacitor applications
ED108	Electrical Properties of Plasma Irradiated Silicon Nanowires for Photovoltaics applications
ED91	Modelling and analysis of single node E-skin piezoresistive pressure sensor simulation results
ED 131	Hydrostatic Pressure Study of GaAsSbN/GaAs Quantum Well Based Optoelectronic Devices
ED132	Performance Analysis of CdTe based PV Array using Parameter Extraction Techniques